ABSTRACT OF THE DISCLOSURE

A back annotation apparatus, which effectively carries out a back annotation, includes: a pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit; a layout pattern verification implementing part for implementing a predetermined layout pattern verification for layout patterns of the logical circuit; a parasitic element extraction part connected to the pre-layout simulation implementing part which extracts parasitic elements from the nodes of which the potential changes; a net list generation part connected to the parasitic element extraction part for generating a net list which includes all the devices included in the layout pattern data and parasitic elements extracted in the parasitic element extraction part; and a post layout simulation implementing part connected to the net list generation part for implementing a post layout simulation by using the net list.